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A Low Power and Low LIR Regulator for Passive RFID Tag in 0.18 μm CMOS Technology

Sajad Nejadhasan, Ebrahim Abiri, Rezvan Dastanian and Mohammad Reza Salehi

Electrical and Electronic Department, Shiraz University of Technology, Shiraz, Iran

ABSTRACT

This paper proposes a low power and low output ripple regulator for radio frequency identification tags. The inner blocks of regulator is supplied from elementary stages output of rectifier. The proposed operational amplifier works on AB class and its bias is in adaptive biasing form. The bandgap reference and sampling voltage resistors used in this paper are completely designed with transistors which culminate in low power dissipation. The regulator output voltage is 1.07 V, while the output ripple is $\pm$1.1 mV. The value of line regulation, power supply rejection ratio, and regulator efficiency are 5.5 mV/V, 45.2 dB, and 71.3%, respectively. A 111 μW power consumption has been calculated with 20 KΩ load. The simulation is done with the help of Cadence software in 0.18 μm CMOS technology, while its operational frequency is 960 MHz. The layout of the proposed regulator is 0.00125 mm^2.

Keywords:
Bandgap reference, LIR, Low power consumption, OPA, Regulator, RFID.

1. INTRODUCTION

The RFID technology is recently improved and has a great development. The passive tag is more considered as it has longer lifetime and lower cost fabrication. For increasing the communication range between tag and reader, low power dissipation circuits are employed.

Figure 1 shows the tag supply block. The transmitted waves from reader are received with tag antenna and are converted into sinusoidal signal. The generated AC signal is converted into DC voltage with the help of voltage regulator. When tag and reader are close to each other, the voltage limiter should be used to ban the damage of tag chip. The rectifier output voltage has probably the ripple which indicates it is not completely rectified. Therefore, a regulator is applied for eliminating ripple. Since different tag blocks need various voltage levels, DC-DC convertor is used. In this paper the regulator block is evaluated.

In reference [1], [2], for decreasing the output voltage ripple of rectifier, first the great ripples of input voltage are diminished with series diode, then this voltage is compared with reference voltage and the output voltage of regulator is produced. The disadvantage of this circuit is the sensitivity to temperature variations. In reference [3], a regulator with low constant current has presented, but its output ripple is big. Reference [4], instead of using two transistors existing in the output sampling voltage circuit, uses MOSFET transistors, in order to decrease chip area. In some of designed regulators [2], [5], the total output voltage is compared with reference voltage which should be comparable with output of regulator. In such designs, the power dissipation of voltage reference circuit is highly increased. In most of the designed reference voltage circuits, one or more bipolar junction transistor (BJT) transistors are employed for the purpose of creating insensitive voltage to temperature [3–6]. But BJT transistors not only have high power consumption but also need high cost for fabrication.

In the proposed regulator, two voltage levels are utilized for decreasing power dissipation. These voltage levels are achieved from the elementary and the extremity rectifier stages. Most of the inner blocks of regulator are supplied with lower voltage and their structure is designed based on this input. The bias of operational amplifier (OPA) block working in AB class is provided with adaptive biasing. These characteristics culminate in low power consumption. In addition using bandgap reference (BGR) which is included only MOSFETs causes more diminishing of power consumption.

The paper is organized as follows: in Section 2, the total structure of the proposed regulator is described. In Section 3, the proposed BGR block is evaluated. In Sections 4 and 5, the designed OPA and sampling voltage resistors are presented, respectively. Finally the simulation results, layout ,and comparison are shown in Section 6.

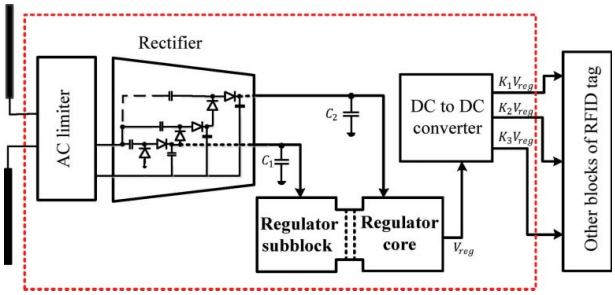

Figure 1: The supply block of RFID tag.

2. THE TOTAL STRUCTURE OF THE PROPOSED REGULATOR

The block diagram of the proposed regulator is shown in Figure 2. It includes three parts; BGR, OPA, and SVR. In this topology, two supply voltages gained from the elementary stage ($V_{\text{in,low}}$) and the extremity stage ($V_{\text{in,high}}$) of the rectifier are employed. In this regulator, the sampled output voltage is compared with reference voltage with the help of OPA block and controls the pass current of transistor $M_{p,\text{pass}}$. If the difference of the R_2 sampled voltage (V_x) and reference voltage (V_{ref}) increases, the OPA output will increase which leads to eliminating the source-gate voltage (V_{sg}) of $M_{p,\text{pass}}$ transistor. Consequently, the drain current of this transistor, which is employed with resistors, is diminished and finally the output voltage is decreased. On the other hand, if $V_x - V_{\text{ref}}$ decrease, the OPA output becomes low and V_{sg} increases. Thus the drain current of $M_{p,\text{pass}}$ transistor is increased which causes the increment of output voltage. Generally, by increasing or decreasing the supply voltage, this circuit produces almost regulated voltage by creating negative feedback loop.

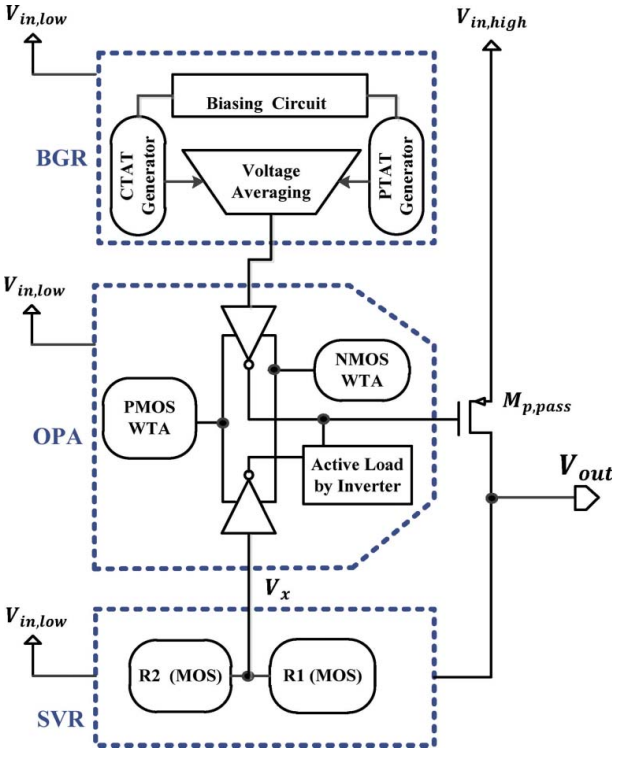

Figure 2: The total block diagram of the proposed regulator.

3. THE PROPOSED BGR

Usually for the realization of the BGR circuit which has low variations by temperature variations, one or more BJT transistors are used to create an independent voltage or current to temperature by the linear combination of V_{BE}, V_T, or ΔV_{BE} which have negative and positive temperature coefficient, respectively. Employing BJT transistors increases the complexity of fabrication process and power dissipation. Therefore, in this paper a completely MOSFET structure of BGR circuit is used.

The proposed BGR is shown in Figure 3. This circuit included four parts: PTAT voltage generator, CTAT voltage generator, voltage average circuit, and insensitive biasing circuit to voltage variations.

The operation of the circuit is as follows: voltage collector block combines PTAT voltage which is proportional to absolute temperature and CTAT voltage which is complementary to absolute temperature and consequently produces independent voltage to temperature.

In the following parts, the different blocks of the proposed BGR is evaluated.

3.1 The Current Source Circuit

In this circuit, a fixed bias current source which is irrespective of supply voltage variation is used. Therefore, the output BGR is insensitive to the supply voltage variation. In this circuit, three N-channel MOSFET (NMOS) transistors, M_{b5}, M_{b6}, and M_{b7}, existing in the bias circuit structure work in sub-threshold region which diminishes power consumption. The current which is produced by two P-channel MOSFET (PMOS) transistors, M_{b3} and M_{b4}, is increased by a temperature rise, therefore NMOS transistors are combined specially to compensate this dependence [7]. The different parts of PTAT and CTAT voltage generators are biased with M_{b1} and M_{b2} transistors of the current source, thus output voltage has low sensitivity to the supply voltage variation.

The startup circuit helps bias current generator to keep its primary state. Based on Figure 3(a), by decreasing bias current or in the other words supply voltage, M_{s1} transistor exert excessive current to the circuit and when the bias current reaches to the desired value, V_{gs} of transistor M_{s1} becomes lesser than V_{th} and turns off to decrease the power consumption.

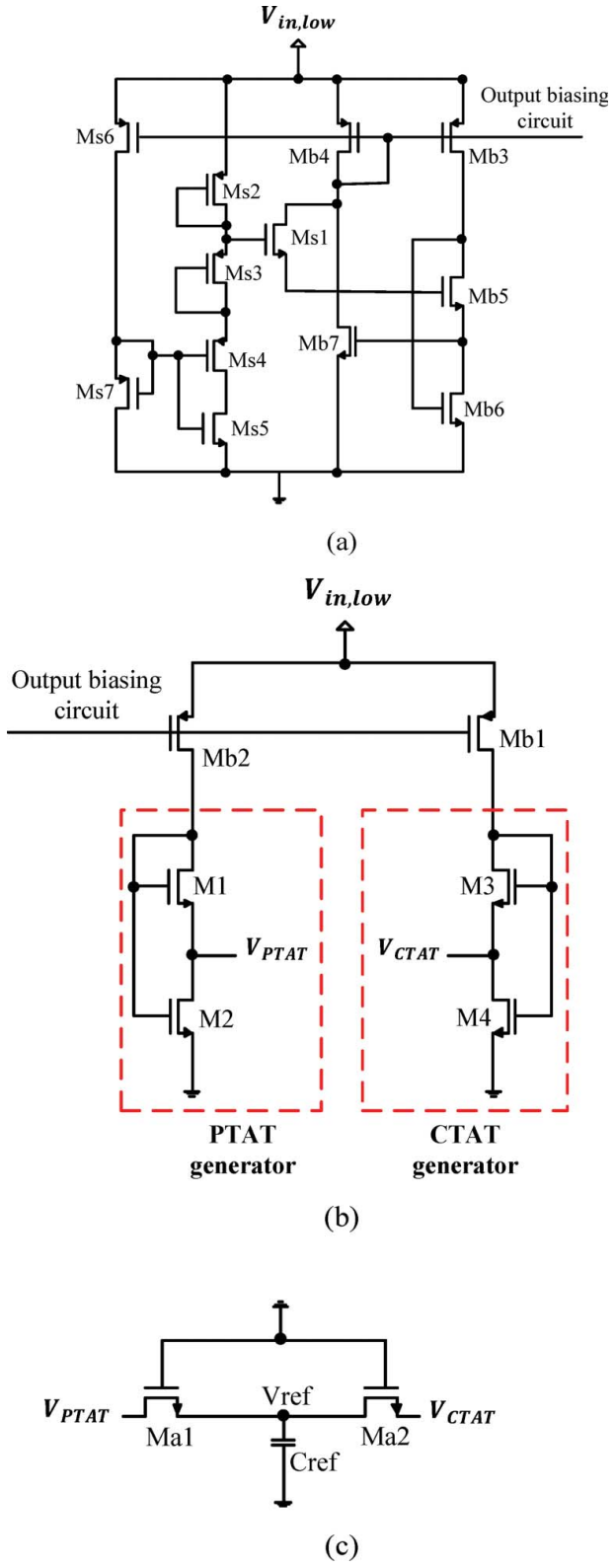

Figure 3: The proposed BGR circuit: (a) the current source circuit, (b) PTAT and CTAT voltage generator, and (c) the voltage averaging circuit.

3.2 The PTAT and CTAT Voltage Generator

The PTAT generator included two connected NMOS transistors, M_1 and M_2, that the output is the difference of two gate-source voltage of transistors [8]. Due to the designed supply voltage of the circuit, transistors work on sub-threshold region, therefore by considering $V_{ds} > 4V_T$, gate-source voltage can be calculated as Eq. (1).

$$V_{gs} = \eta V_T \ln\left(\frac{I}{I_s\left(\frac{W}{L}\right)}\right) + V_{th} \tag{1}$$

If the proportion of W/L of transistor M_1 to that of transistor M_2 equals to K ($K > 1$), the difference of two gate-source voltages is calculated from Eq. (2). With due attention to the positive temperature coefficient of V_T, by increasing the temperature, this voltage difference, which is considered as V_{PTAT}, is increased.

$$V_{PTAT} = V_{gs2} - V_{gs1} = \eta V_T \ln(K) \tag{2}$$

Similarly, if the proportion of W/L of transistor M_4 to that of transistor M_3 equals to K' ($K'>1$), V_{CTAT} can be calculated from Eq. (3).

$$V_{CTAT} = V_{gs4} - V_{gs3} = -\eta V_T \ln(K') \tag{3}$$

In order to decrease CTAT voltage by increasing temperature proportional to the increment of PTAT voltage, the structure like PTAT circuit is used and the value of W/L for M_3 and M_4 transistors is set in order to produce insensitive voltage to temperature by combining PTAT and CTAT voltages.

3.3 The Voltage Averaging Circuit

For combining two PTAT and CTAT voltages, the voltage averaging circuit, which is shown in Figure 3(c), is used. With this simple configuration, the average of two produced voltage is achieved in the output.

In this circuit, the characteristics of inner capacitors of transistors are used. The simplified capacitance structure of the proposed voltage averaging circuit is shown in Figure 4 and the equal capacitance of it is presented in Table 1.

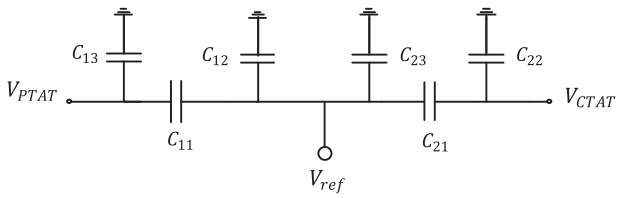

Figure 4: The simplified capacitance structure of the proposed voltage average circuit.

Table 1: The equal capacitors of Figure 4

C_{11}	C_{12}	C_{13}	C_{21}	C_{22}	C_{23}
C_{DB1}	$C_{GB1} \mid\mid C_{GS1}$	C_{GD1}	C_{DB2}	$C_{GB2} \mid\mid C_{GS2}$	C_{GD2}

In this structure, since the body of transistor is connected to its source, the body-source capacitor is omitted. C_{GD}, C_{GB}, C_{GS}, and C_{DB} are the capacitor between gate and drain, the capacitor between gate and base, the capacitor between gate and source, and the capacitor between drain and body of M_{a1} and M_{a2}, respectively.

By analyzing Figure 4, Eq. (4) is obtained. Based on this equation, the output voltage is the weight combination of PTAT and CTAT voltages.

$$V_{\text{ref}} = \frac{C_{11}}{C_{11}+C_{12}+C_{21}+C_{23}} V_{\text{PTAT}} + \frac{C_{21}}{C_{11}+C_{12}+C_{21}+C_{23}} V_{\text{CTAT}} \quad (4)$$

Due to Eqs. (5) and (6), if M_{a1} and M_{a2} transistors have similar structures and the combination of PTAT and CTAT voltages is fixed during the desired temperature range, C_{11} and C_{21} will be same.

$$C_{DB1} = \frac{C'_{j1}}{(1-\frac{V_{DB1}}{\Phi_{j1}})^m} A_{D1} + \frac{C'_{\text{jsw1}}}{(1-\frac{V_{DB1}}{\Phi_{\text{jsw1}}})^m} P_{D1} \quad (5)$$

$$C_{DB2} = \frac{C'_{j2}}{(1-\frac{V_{DB2}}{\Phi_{j2}})^m} A_{D2} + \frac{C'_{\text{jsw2}}}{(1-\frac{V_{DB2}}{\Phi_{\text{jsw2}}})^m} P_{D2} \quad (6)$$

where A_D and P_D are the drain area and the drain perimeter of M_{a1} and M_{a2} transistors, respectively. Φ_j is the built-in junction potential and Φ_{jsw} is the sideband wall potential. C'_j and C'_{jsw} are calculated as Eq. (7).

$$C'_j = \sqrt{\frac{\varepsilon_{si} q N_B}{2\Phi_j}}, \quad C'_{\text{jsw}} = \sqrt{\frac{\varepsilon_{si} q N_B}{2\Phi_{\text{jsw}}}} \quad (7)$$

where ε_{si} is the silicon dielectric constant and N_B is the body impurity.

Given the fact that the value of C_{23} capacitor, the whole capacitor between gate and drain, is lower than the other capacitors, it can be neglected. Therefore, the output voltage is gained from Eq. (8).

$$V_{\text{ref}} = \frac{C_{11}}{2C_{11}+C_{12}} V_{\text{PTAT}} + \frac{C_{11}}{2C_{11}+C_{12}} V_{\text{CTAT}} \quad (8)$$

Since $C_{12} >> C_{11}$, the BGR can be simplified as Eq. (9), that the output is the average of two PTAT and CTAT voltages.

$$V_{\text{ref}} = \frac{V_{\text{PTAT}} + V_{\text{CTAT}}}{2} \quad (9)$$

As the oscillator is not used in the averaging circuit, this circuit has less complexity and lower power consumption compared to the other circuits [8], [9].

4. THE PROPOSED OPA

The complete designed OPA block is shown in Figure 5. This circuit consists of three parts: circuit core, two adaptive biasing blocks PMOS WTA and NMOS WTA, and an active load.

4.1 OPA Circuit Core

The differential amplifier inputs of the proposed OPA core circuit shown in Figure 5(a), are in the form of inverter. With the help of this structure, a low current dissipation and high gain can be achieved. The result of increasing gain in this topology is the combination of transconductance of n and p type MOSFET which is presented in Eq. (10).

$$G_m = G_{\text{mn}} + G_{\text{mp}} \quad (10)$$

Therefore based on this equation the gain increases appropriately [10]. One of the disadvantages of this circuit is the low bandwidth, as a result of low bias current in inverter amplifier. This problem is solved with adaptive biasing blocks.

4.2 Adaptive Biasing Blocks

The confined biasing currents confine the maximum output current which results in decreasing the gain. On the other hand, using high biasing current leads to increasing the power consumption. For solving this problem, the adaptive biasing blocks are employed for biasing the amplifier in the proposed design. In this circuit, when the excess input is employed, the biasing current is automatically increased. Due to Figure 5(b), NMOS WTA and PMOS WTA are used as the adaptive biasing for NMOS and PMOS transistors of inverter, respectively [11], [12].

If the input voltages are same and equal to common mode voltage ($V_{\text{ref}} = V_{\text{x}} = V_{\text{cm}}$) and the biasing current is equal to I_B.

The output of PMOS WTA is based on the larger value of input voltage as follows. If V_{ref} is more than V_x, the source-gate voltage of M_{w4} transistor is increased, therefore the drain voltage is accelerated and M_{w4} transistor enters to triode region. Thus the voltage of node

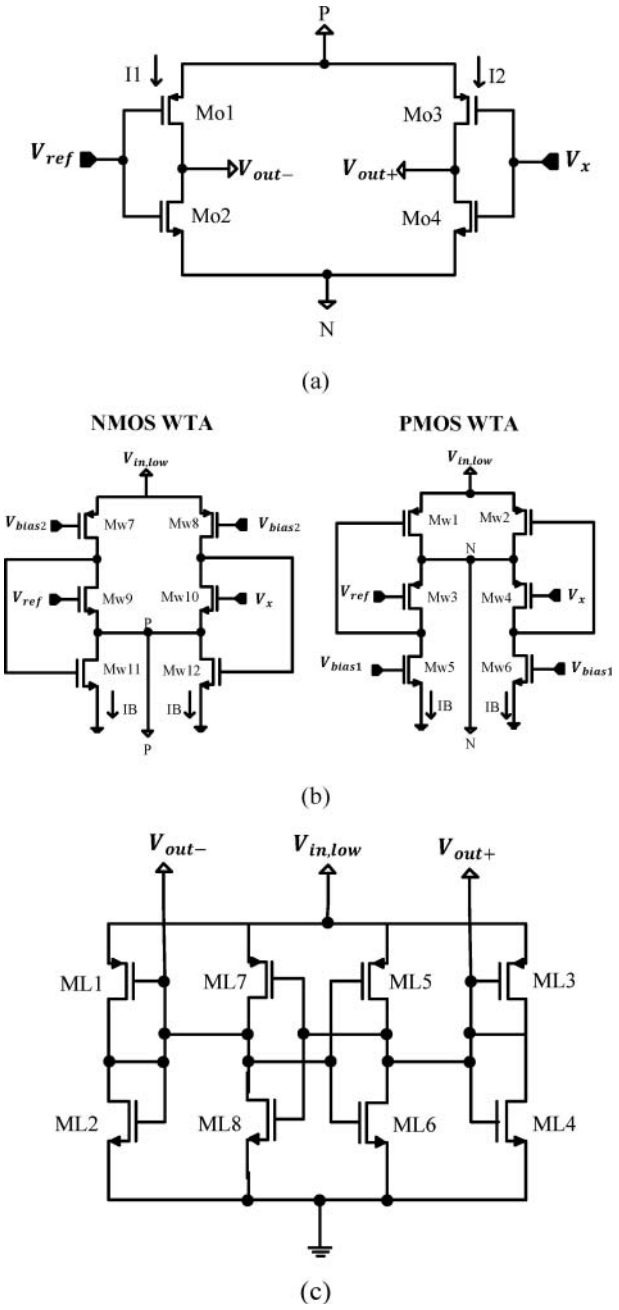

Figure 5: The total circuit of the proposed OPA: (a) OPA circuit core, (b) adaptive biasing blocks and (c) output active loads as inverter.

N is determined by V_{ref} and M_{w3} transistor which is same as Eq. (11).

$$V_N = V_{\text{ref}} + V_{\text{gs},Mw3} \tag{11}$$

Under this condition, I_2 current is much more than I_B current and I_1 is equal to I_B. In addition, if V_x is greater than V_{ref}, V_N can be calculated as Eq. (12) and I_1 is much more than I_B. In this case I_2 is same as I_B.

$$V_N = V_x + V_{\text{gs},Mw4} \tag{12}$$

The NMOS WTA output biasing the NMOS transistors of the invertors, is based on the smaller value of input voltage, while same analysis like the one for PMOS WTA can be done. Consequently, by using adaptive biasing circuits, the pass current of inverter amplifier transistors can be increased as high gate-source voltage is created, so the bandwidth and the gain of amplifier are improved.

4.3 The Output Active Loads as Inverter

The active load shown in Figure 5(c), consists of four inverters [10]. Two innermost inverters (M_{L5}-M_{L8}) have the cross-coupled structure. Such connections create positive feedback which generates negative resistor with the value of -2/g_{mi}, in which g_{mi} is the transconductance of innermost inverters. Two outermost inverters (M_{L1}-M_{L4}) which are connected as diode connected, create positive resistor with the value of 2/g_{mo}, in which g_{mo} is the transconductance of the outermost inverters. By combining these two resistors, inherent instability achieved by negative resistor is eliminated. If innermost and outermost inverters coincide with each other, the great output impedance is gained which culminates in high amplifier gain.

5. THE CONFIGURATION OF VOLTAGE SAMPLING RESISTORS BY MOSFET

Using common resistors in regulator structure increases not only power consumption, but also the chip area. Therefore, two transistor configurations are replaced sampling voltage resistors. In this condition, a NMOS diode connected transistor is replaced R_1 resistor of Figure 2. Instead of R_2 resistor, the circuit shown in Figure 6 is used which is a voltage-controlled grounded resistor [13]. In Figure 6, M_{R2} transistor works in triode region and its equal resistor can be calculated as Eq. (13).

$$R_2 = \frac{V_{\text{DS}}}{I_D} = \frac{1}{k(V_{\text{GS}} - V_{\text{th}} - \frac{V_{\text{DS}}}{2})} \tag{13}$$

V_{DS} parameter in this equation is nonlinear. This parameter is omitted with $M_{r1} - M_{r6}$ transistors which have a voltage collector structure and are biased in saturation region. Due to the same drain currents of $M_{r1} - M_{r4}$ transistors and currents of M_{r5} and M_{r6} transistors, V_o voltage, which is employed to the gate of M_{R2} transistor, can be calculated as Eq. (14).

$$V_o = \frac{V_x}{2} + V_c + \frac{V_{\text{in,low}}}{2} \tag{14}$$

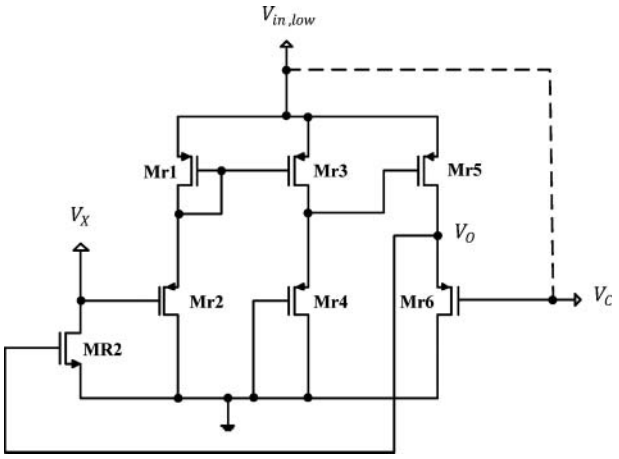

Figure 6: The voltage-controlled grounded resistor.

By employing this voltage to the gate of M_{R2} transistor, R_2 resistor has no nonlinear terms and based on Eq. (15) it can be controlled by V_c voltage.

$$R_2 = \frac{1}{k(V_c - V_{\text{th}} + \frac{V_{\text{in,low}}}{2})} \tag{15}$$

By changing V_c, different values for R_2 can be achieved. In the proposed regulator, the controlled voltage for this resistor is gained from $V_{\text{in,low}}$. Given the fact that the voltage-controlled grounded resistor uses one controlled voltage, it has lower power dissipation in compare with the other grounded resistors.

W/L of pass transistor ($M_{p,\text{pass}}$) and NMOS transistors used for R_1 and R_2 resistors, should be appropriately selected for the desired output voltage to decrease the input voltage ripple. Also their dimensions should be correctly chosen that the chip area is not highly increased.

6. SIMULATION RESULTS

6.1 BGR Simulation Results

Figure 7 shows the variation of PTAT, CTAT, and output voltages versus temperature in the range of −40 °C to 130 °C. For the designed regulator, the BGR is set to 50 mV.

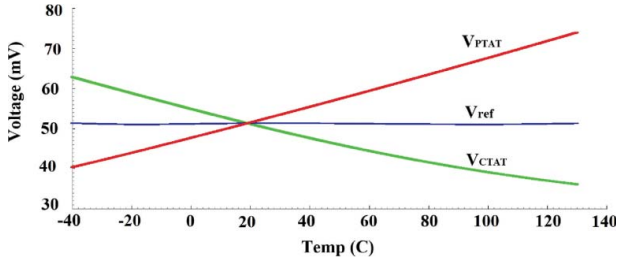

Figure 7: The variation of PTAT, CTAT, and V_{ref} with temperature.

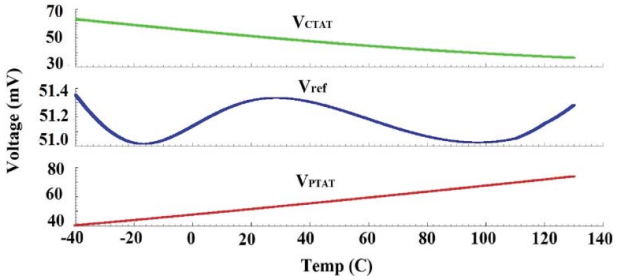

Figure 8: The variation of PTAT, CTAT, and V_{ref} with temperature, in separate form.

PTAT, CTAT, and V_{ref} voltages are shown in Figure 8 more precisely. It can be clear that the variation of output BGR for this range of temperature is about 0.34 mV, while the temperature coefficient based on Eq. (16) is 40 ppm/°C.

$$\text{TC} = \frac{V_{\max} - V_{\min}}{V_{\text{out}}(T_{\max} - T_{\min})} = 40\,\text{ppm/°C} \tag{16}$$

Figure 9 shows the DC analysis for output voltage variations versus supply voltage in the range of 0.4 to 1 V. In this range, the variation of output voltage is about 4.14 mV.

The current variations and power consumption of the proposed BGR versus the variation of DC input are shown in Figure 10. The power consumption for the minimum and maximum employed voltage (0.4 and 1 V) is 0.355 and 178 nW, respectively. The power dissipation for 0.5 V voltage, is 1.1 nW.

Table 2 compares the proposed BGR circuit with the other designed circuits.

As it is clear, the proposed BGR has not only lower temperature coefficient but also lower power dissipation

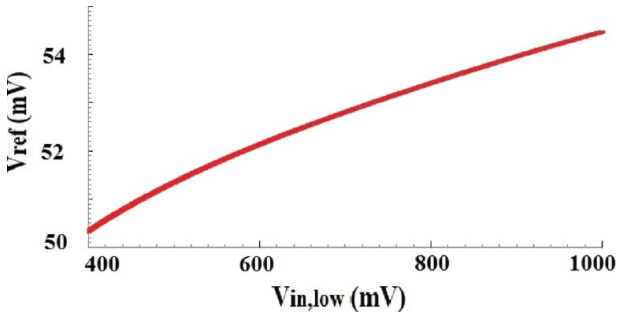

Figure 9: The output voltage variation versus supply voltage.

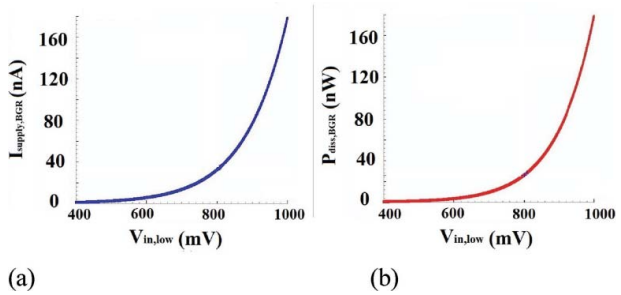

Figure 10: The variation curves of (a) current consumption, (b) power consumption, for the proposed BGR circuit versus input DC voltage.

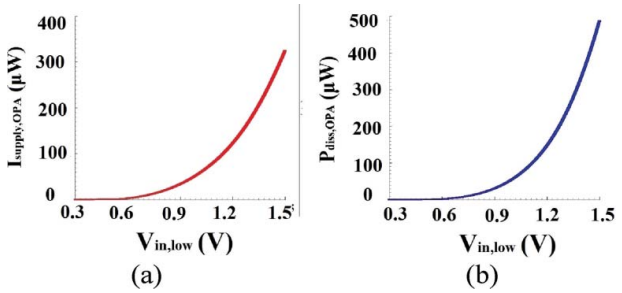

Figure 11: The variation curves of (a) current consumption, (b) power consumption, for the proposed OPA circuit versus input DC voltage.

and chip area, in comparison with the other BGR circuit. The proposed BGR with lower supply voltage generates fixed output for various temperature and different input DC voltages, which is suitable for RFID applications.

6.2 OPA Simulation Results

The variation of current and power dissipation of the proposed OPA, versus the variation of input DC voltage is shown in Figure 11. The current and power consumption for different inputs are presented in Table 3. As it is obvious, decreasing supply voltage effects on decreasing power consumption of the OPA, because by decreasing the supply voltage, transistors work on subthreshold region. For 0.5 V supply voltage, the power dissipation of the OPA is 534.5 nW.

Table 3: The power and current consumption of the proposed OPA circuit for various inputs

V_{in}	I_{supply}	$P_{consumption}$
0.4 V	291.5 nA	116.6 nW
0.5 V	1.069 μA	534.5 nW
0.7 V	8.525 μA	5.967 μW
1 V	54.93 μA	54.93 μW
1.5 V	324.5 μA	486.8 μW

6.3 Simulation Voltage Controlled Grounded Resistor

The current- voltage curve of R_2 is shown in Figure 12 for three V_c values. For large negative V_c voltage, the resistor is more than 20MΩ.

6.4 Simulation Results of the Proposed Regulator

Figure 13(a) shows the transient response simulation result of the regulator output. In this simulation, the input voltage frequency is assumed 960 MHz, while inputs which are achieved from the elementary and the extremity stage can be calculated as Eqs. (17) and (18).

$$V_{\text{in,low}} = 0.5 + 0.05\sin(2\pi \times 960 \times 10^6 t) \quad (17)$$

$$V_{\text{in,high}} = 1.5 + 0.2\sin(2\pi \times 960 \times 10^6 t) \quad (18)$$

Although the disturbances with 165 and 500 mV amplitude are employed to $V_{\text{in,low}}$ and $V_{\text{in,high}}$, the output of the regulator is still fixed as shown in Figure 13(b).

Output voltage is 1.07 V which its ripple is about ±1.1 mV. The input voltage, the output voltage, the voltage of R_2 resistor (V_x), and the V_{ref} voltage are shown together in Figure 14.

By considering 1.5 V for input voltage, 20 KΩ for load resistor and 4pF for load capacitor, the total power consumption is equal to 111 μW.

Table 2: The comparison of the proposed BGR parameters with the ones of other BGR circuits

	This work	[7]	[9]	[14]
Process (μm)	0.18	0.18	0.18	0.18
Supply voltage (V)	0.4 to 1	0.6 to 2	0.45 to 2	0.6 to 2.3
Current (nA) @ Supply voltage (V)	2.2 @ 0.5 178 @ 1	32 @ 0.6 102 @ 1.8	7 @ 0.45 8 @ 1.8	<40 @0.7 –
V_{ref} (mV)	50	222	263.5	220
TC (ppm/C)	40	135	142	127
T range (C)	[−40:130]	[−25:125]	[0:125]	[−20:100]
PSRR (dB)	−43	−52	−12.2	−41
Freq (Hz)	960M	1M	≥10M	100
Area (mm^2)	0.00044	0.015	0.0430	0.0040

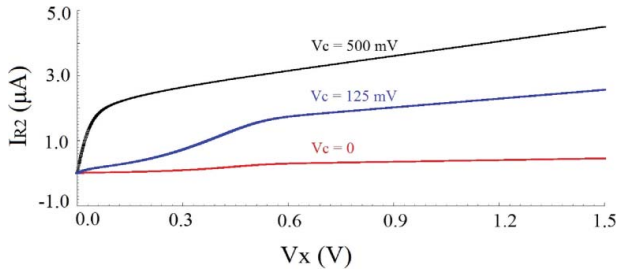

Figure 12: The current-voltage curve of R_2 for three values of V_c.

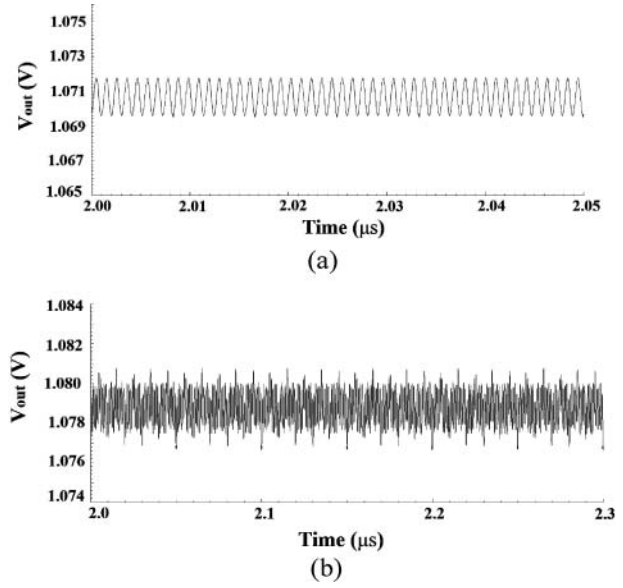

Figure 13: The output voltage of the proposed regulator (a) without distortion (b) with distortion.

The effect of the mismatch and the process variation on the proposed regulator output represents the mean and the standard deviation about 1.065 V and 24.16 mV, respectively, for 500 runs of Monte Carlo which is shown in Figure 15.

The layout of the proposed regulator shown in Figure 16, represents 0.00125 mm^2 chip area.

Table 4 shows the comparison of the proposed circuit with three other regulators. As it is clear, by comparing

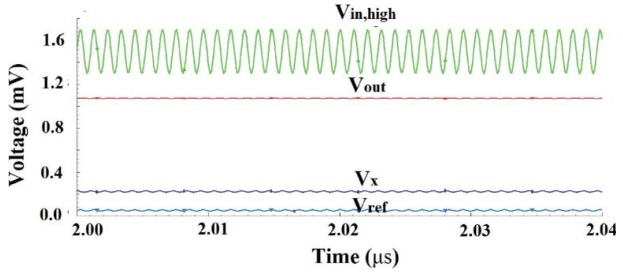

Figure 14: The input voltage, output voltage, V_x and V_{ref} together at the same curve.

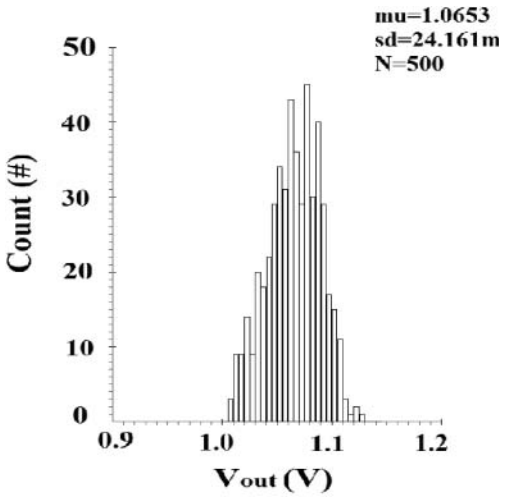

Figure 15: The effect of the mismatch and the process variation on the proposed regulator output.

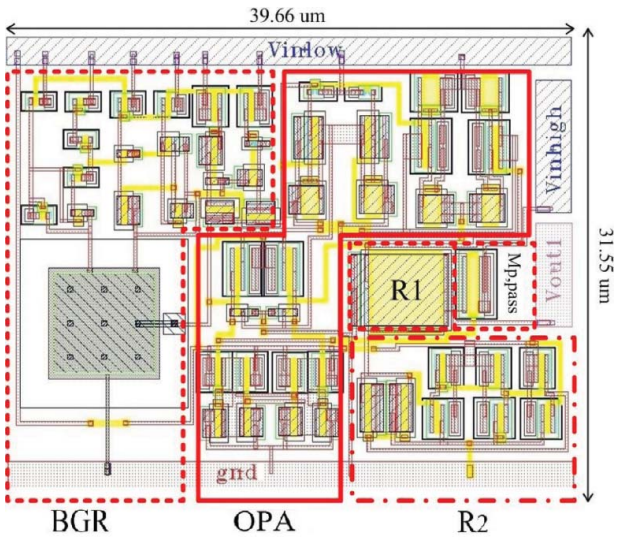

Figure 16: The layout of the proposed regulator which its size is 0.00125 mm^2.

Table 4: The comparison of the proposed regulator parameters with the ones of the other circuits

	This work	[5]	[15]	[16]
Technology (μm)	0.18	0.35	0.18	0.35
V_{in} (V)	1.5 & 0.5	2.2	–	3
ΔV_{in} (mV)	400 & 100	–	400	–
V_{out} (V)	1.07	1	1.5	0.605
ΔV_{out} (mV)	2.2	–	7	–
Efficiency	71.3%	45.45%	–	20%
I_L (mA)	0.05	0.5	–	0.005
$I_{quiescent}$ (μA)	28	35.5	–	0.034
PD (mW)	0.111	1.2	–	0.015
LIR (mV/V)	5.5	39	12	–
PSRR (dB)	−45.2	−38	−35.1	−58.5
Freq (MHz)	960	10	1	2
Chip area (mm^2)	0.00125	–	–	–

the load, power consumption, voltage efficiency and LIR, the proposed regulator has better operation than the other references.

7. CONCLUSION

In this paper, a regulator circuit working at 960 MHz frequency is presented for RFID tag. For supplying the circuit, two voltage levels, 0.5 and 1.5 V, which are gained from the elementary and the extremity stage of the rectifier, are used. For decreasing the power consumption, sub-blocks are supplied with 0.5 V. By using adaptive biasing for OPA and total MOSFET structure for regulator, the power consumption and chip area are decreased. The power consumption of the circuit for 20 KΩ load resistor is about 111 μW, while its chip area is 0.00125 mm^2. The sinusoidal input voltage ripple for $V_{\text{in,low}}$ and $V_{\text{in,high}}$ are considered 100 and 400 mV, respectively. Due to these assumptions for simulation, the output voltage is achieved 1.07 V with ±1.1 mV ripple. The LIR and PSRR are 5.5 mV/V and -45 dB, respectively.

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Authors

Sajad Nejadhasan was born in Iran, Bushehr, in 1987. He received the BSdegree in the Department of Engineering from Persian Gulf University in 2011 and is currently working toward the MSc degree in electrical engineering at Shiraz University of Technology (SUTECH). His research interests include design of power management block in RFID tags.

E-mail: s.nejadhasan@sutech.ac.ir

Ebrahim Abiri received the BSc degree in electronics engineering from Iran University of Science and Technology (IUST) in 1992, MSc degree from Shiraz University in 1996 and the PhD degree in electronics from Iran University of Science and Technology (IUST) in 2007. He has authored more than 50 published technical papers in electronics and power electronics and four books. He has been with the Department of Electrical Engineering, Shiraz University of Technology (SUTECH), since 2007. His current research activities include analog circuit design and power electronic.

E-mail: abiri@sutech.ac.ir

Rezvan Dastanian was born in Iran, Ahvaz, in 1986. She received the BSc and MSc degrees in electrical engineering from Iran University of Science and Technology (IUST), Iran, Tehran in 2008 and 2011, respectively and is currently working toward the PhD degree in electrical engineering at Shiraz University of Technology (SUTECH). Her research interests include RFIC design, low power circuit design, sensor, DC-DC converter, and microelectronics.

E-mail: r.dastanian@sutech.ac.ir

Mohammad Reza Salehi received the BSc degree in electrical engineering from Amirkabir University of Technology (Tehran Polytechnique), Tehran, the MSc degree in electrical engineering from Shiraz University, Shiraz, Iran, and the PhD degree in optoelectronics at the ENSERG/INPG, France. He has authored and co-authored over 70 journal and conference papers and seven books. He is currently a member of IEEE. His research interests include optoelectronics, optomicrowaves and optical systems.

E-mail: salehi@sutech.ac.ir

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